

FPG 19-01-01

PULSE PATTERN GENERATOR



The FPG 19-01-01 is a pseudo random pulse pattern generator typically capable of operation up to 2.7 Gb/s. It provides a fast rise time and low pulse distortion. The unit can accommodate two internal clock generators and also supports an external clock input. It provides a clean pulse output suitable for applications such as optical communications, fast pulse amplifiers and high speed logic circuits development.

Typical operation to 2.7 Gb/s

50 ps rise and fall times

5 % overshoot

1 vpp output amplitude

Low noise internal clocks

Low cost



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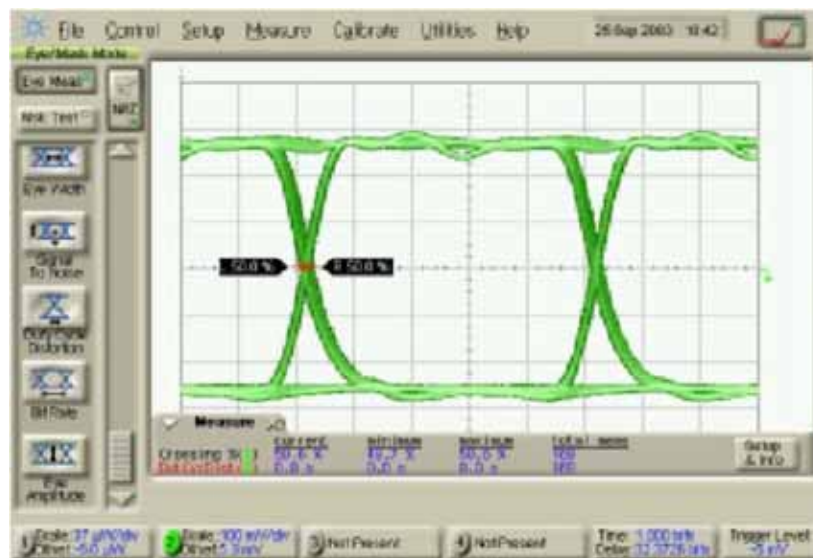
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Electrical Specification

Parameter	Units	Min	Typ	Max
Operating frequency				
Internal clock 1 (factory set) ¹	GHz	0.1	-	2.7
Internal clock 2 (factory set) ¹	GHz	0.1	-	2.7
External clock ²	GHz	0.1	-	2.7
External clock				
Input level	V _{pp}	0.3	-	1.5
Rise time	Ns	-	-	1
Internal clock				
Stability	ppm/°C	-	0.3	1
SSB phase noise (10 kHz offset)	dBc/Hz	-	-120	-
Pseudo random binary sequence				
Pattern length ³ (2 ⁿ -1)	n	-	7,10,15	-
Mark ratio	-	-	1/1	-
Data output ^{4,5}				
Amplitude (50 Ω load)	V _{pp}	0.9	1.0	1.1
Rise/Fall time (20% to 80%)	ps	-	50	60
Jitter	ps	-	18	30
Overshoot	%	-	5	10
dc Bias injection (BNC connector)				
dc current	mA	-100	-	100
dc voltage	v	-15	-	+15
dc resistance	Ω	10	14	16
3 dB bandwidth ⁶	kHz	10	20	-
Clock output ⁴				
Amplitude	V _{pp}	0.3	0.4	0.8
Rise/fall time(20% to 80%)	ps	-	120	200
Clock/16 output ⁴				
Amplitude	V _{pp}	0.7	0.9	1.2
Rise/fall time (20% to 80%)	ps	-	120	800
Pattern sync output ^{4,7}				
Amplitude	V _{pp}	0.7	0.9	1.2
Rise/fall time(20% to 80%)	ps	-	120	800
Operating temperature range	°C	+10	-	+35
Power	Selectable AC 110-120v (60Hz), and 220-240v (50Hz), <25VA			
Weight	<3kg			
Notes	<ol style="list-style-type: none"> Internal clock(s) are fixed frequency set during manufacture Maximum external clock frequency typically up to 2.7GHz User selectable patterns, 2⁷-1 and 2¹⁵-1 in accordance with CCITT All data and clock inputs and outputs have SMA connectors Data output is non return to zero(NRZ) 50 Ω Load connected to data output Pattern sync only on 2⁷-1 pattern length 3 Sigma measurement 			

The FPG19-01-01 provides a pseudo random binary sequence (PRBS) synchronised to either an internal or external clock. It provides three types of synchronisation output signals, Clock, Clock/16, and Pattern. The clock is a square wave with a typical amplitude of 0.7 vp p. The clock/16 is derived from the clock signal by means of low noise dividers. The typical amplitude of this is 1 vp p . The pattern synchronisation output produces an output synchronised to the length of the PRBS sequence selected. This allows, for example, the individual data bits to be observed on a sampling oscilloscope. It is available on the 27 -1 pattern length setting.



2.488Gbps eye diagram

The data output provides a 1 vp p signal with fast transitions of 50 ps. The output level can be boosted externally using one of Anritsu wideband amplifiers. For example, the FPG32-01-01 will provide an output of 6.5 vp p into 50 W with a typical rise time of 80 ps. A dc offset can be added to the data output of the FPG19-01-01 by means of an internal bias-T. This can handle a maximum dc voltage of +16 v at +100 mA. At high bias currents, a voltage drop will occur due to the internal dc resistance of the bias-T. This is typically 14 W.