PHYTREX
Innovative Transmission Tech

FMTS-PON

Burst Mode Tester

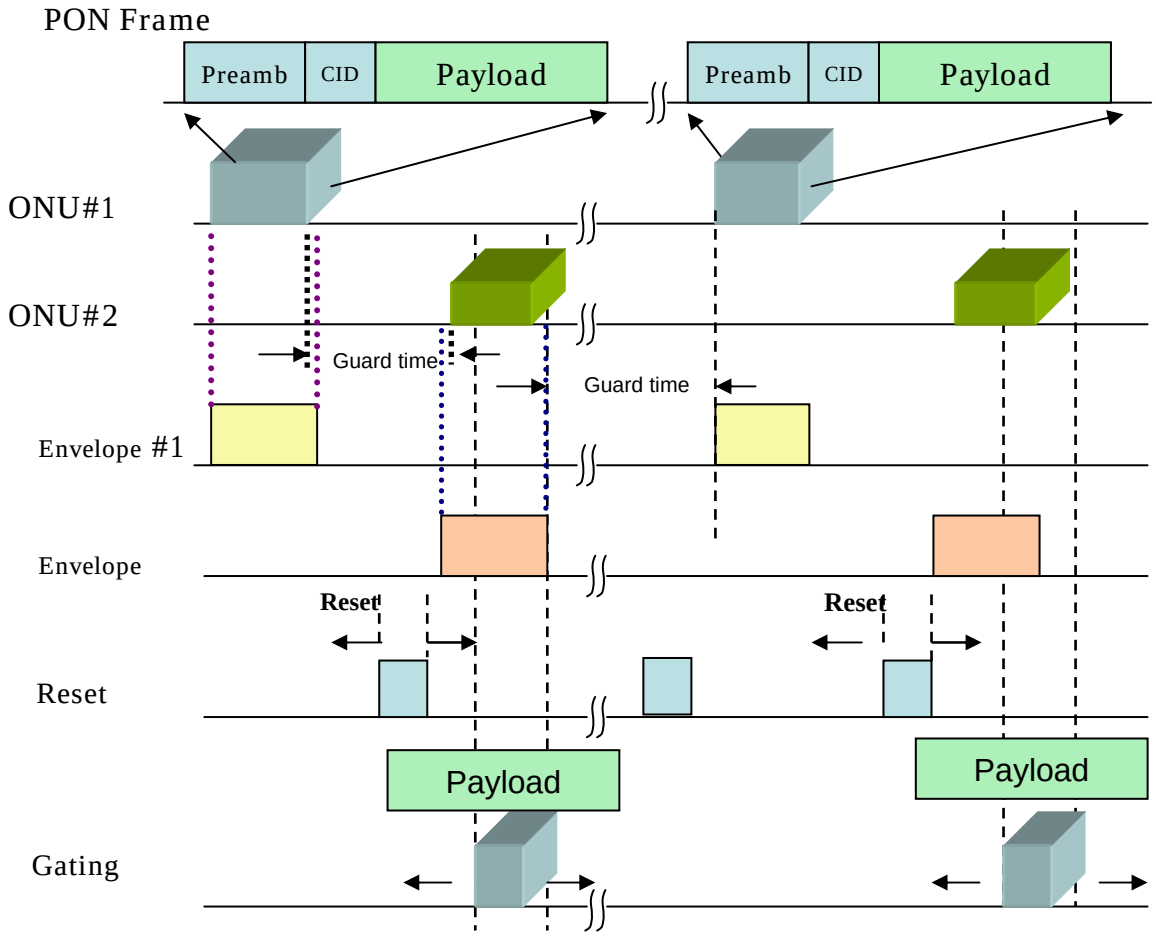
Technical Specification

Introduction

FMTS-PON is the testing instrument which is fully specified designed for PON(Passive Optical Network) subscriber TDM/TDMA transmission architecture.(Figure 1) It can simulate two operation modes, downstream transmission to ONU and upstream transmission to OLT and operating speed (frequency) is from 155Mb/s to 1.25 Gb/s. FMTS-PON can be applied on B-PON, E-PON and G-PON measurements. Under the upstream mode, two burst data signals are emitted, and they are derived into two optical signals through E/O converter. Then, the power level is degraded using an optical attenuator, and, finally, two signals are combined into one signal stream using a 50% coupler.

Burst cycle, **guard time**, **preamble** and **data length** could be adjusted while setting up the burst packet under the upstream mode.

Figure 1：Burst data applied on Upstream PON module test：



FMTS-PON cooperates with Anritsu MP1763C utilizing the rear 8 channels to generate the PON pattern and relative timing sequences. Furthermore, Anritsu MP1764C can be applied for error detection depending on the receiver bit rate of OLT.

Features

Separating Evaluation Board

FMTS-PON provides two ONU and one OLT boards which are independent from the system mainframe. Customers can replace the TRX module into their DUTs to evaluate the performance. Under this architecture, FMTS-PON not only can measure the performance of OLT but also qualify the performance of burst transmitting on each ONU.

Upstream/Downstream measurement

FMTS-PON can support upstream (ONU→OLT) and downstream(OLT→ONU) operation modes from the control system panel. Under downstream mode, continuous data stream will be generated from the OLT side and broadcasted to each ONU through a optical splitter. For upstream mode, operator can self define the structure and the sequence of burst packet, and provides very flexible condition to meet various measurement configurations.

PON Frame Structure

From the ITU-T Recommendation G.983.1/3,the receiver performance of OLT should be guaranteed at least -30dBm power level with specified 1E-12 BER. The testing pattern should be conformed the condition of the standard. FMTS-PON upstream testing frame structure consists of Preamble(PR) bits、Delimiter bits、Consecutive Identical Digits(CID) bits and Information bits three parts, and they are fully compatible to the requirements of standard .(Figure I)

Pattern

This provides multiple testing patterns to enrich the operator to verify the variable applications. PRBS : 7, 23 ; All 0, All 1, User define pattern (PRGM) could be up to 65K bits, Compliant random test pattern (CRPAT) and Compliant Jitter test pattern (CJTPAT) which was defined by IEEE.

Variable **T**iming **C**ontrol (Upstream mode)

FMTS-PON upstream mode provides several kinds of timing signals which are applied on ONU Tx, including two data channels, its relative laser enable/disable timing control signals, a reset signal for DUT receiver circuit to identify the gap between two burst packets and a gating signal for measuring sensitivity.

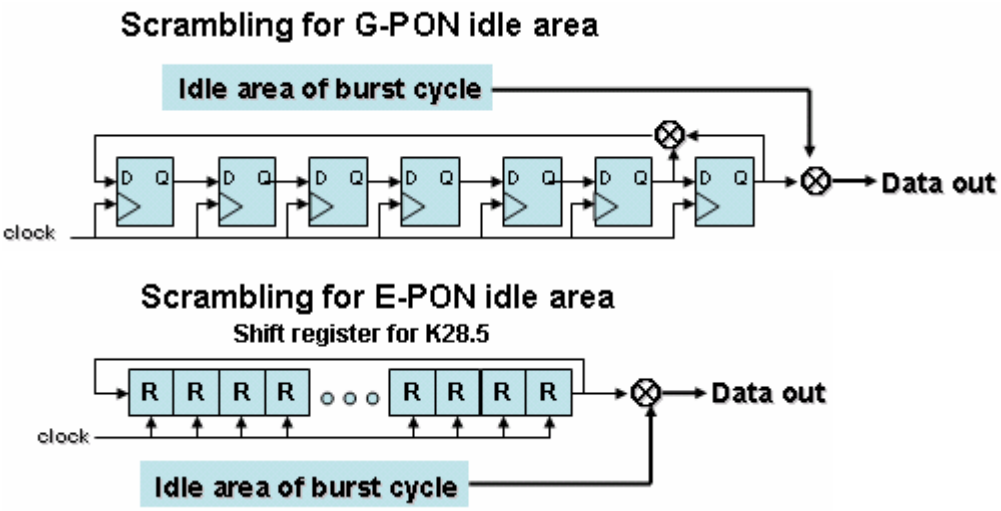
Auto **G**ating **A**lignment (Upstream mode)

One of the most powerful features of FMTS-PON upstream mode is to provide automatically or manually alignment mechanism on serial input data stream from DUT. From the control panel, user can specify the desire portion of the PON frame signal before input the **B**it **E**rror **R**ate **T**ester (BERT). Gating range will auto align and synchronize the pattern inside Error Detector.

Scrambler

To keep the DC balance under digital transmission system, FMTS-PON provides two different coding algorithms ,X^7 + X^6 + 1 and K28.5 to scrambling the idle area of burst

packet transmission. The operator can check the mark density from the system to verify influence by the DC threshold drift for optical transmission caused by the content of pattern.



Virtual **C**hannel **E**mulation (Upstream mode)

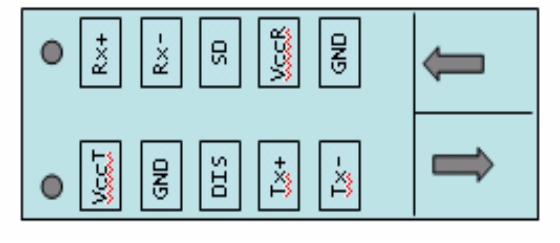
FMTS-PON provides not only two authentic upstream channels, but also emulate up to tree times of original physical channels for testing. Under this system, it can generate up to six various burst channels simultaneously to evaluate the performance of OLT receiver.

Save/**R**ecall

The system also provides save/recall function to simplify setting procedure. User can save/recall the system configuration and graphical / numerical data results also can be exported.

Testing Fixture:

FMTS-PON's evaluation boards are the perfect vehicle for testing and evaluation for optical transceivers and components. The board consists of the plug in sockets, high speed SMA connectors, laser enable control interface, signal detect (SD) , and digital diagnostic monitoring function (option). The signal detect is a single-ended +3.3V TTL compatible output and threshold is set to transition from high to low state between assert and de-assert power range.



PIN assignment for ONU/OLT EV board

PIN	Description
VccT/ VccR	Tx/Rx power supply (+3.3V). Embedded the power supply filter circuit
GND	Connect to ground plane
SD	Signal Detect.
DIS	Connect this PIN to +3.3 TTL logic to control Laser turn on/off.
Tx+/- Rx+/-	Transmitter/Receiver Differential Data Input/Output (50ohm to +1.3V)

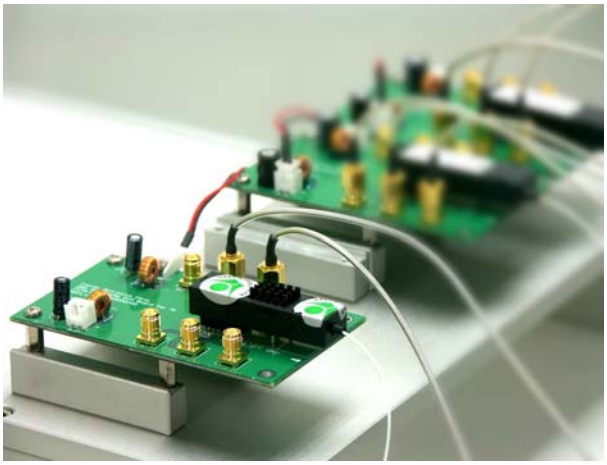


Figure 2 Optical Module & EV Boards

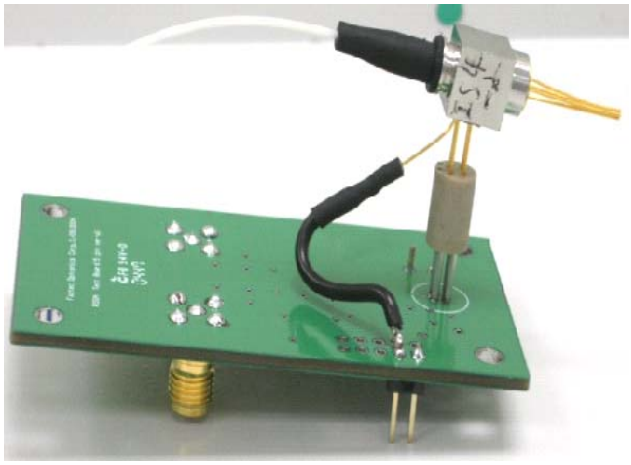


Figure 3 OLT BIDI Testing Fixture

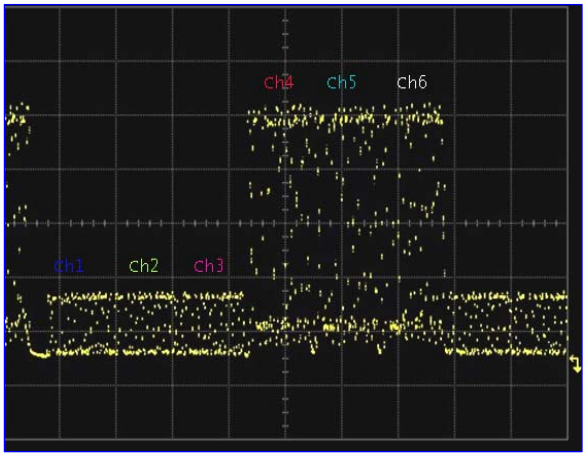


Figure 5、 Six ONU Channels

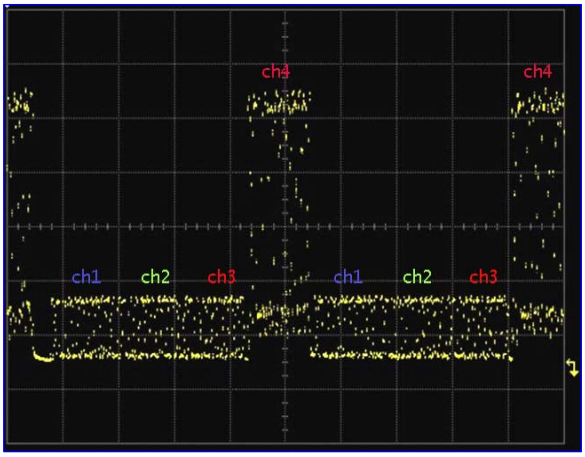


Figure 6、Four ONU Channels

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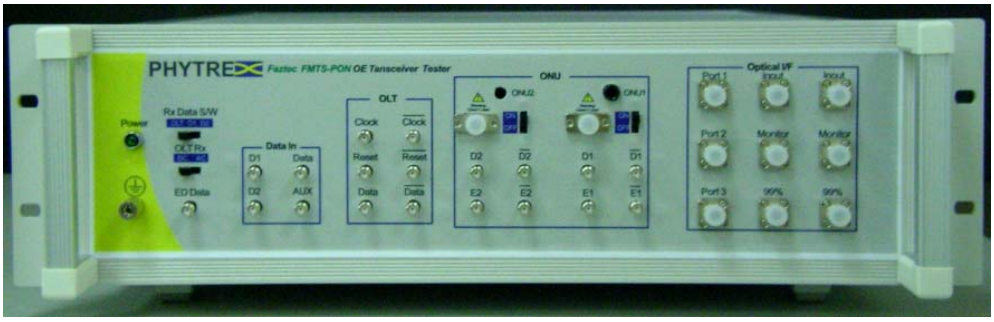
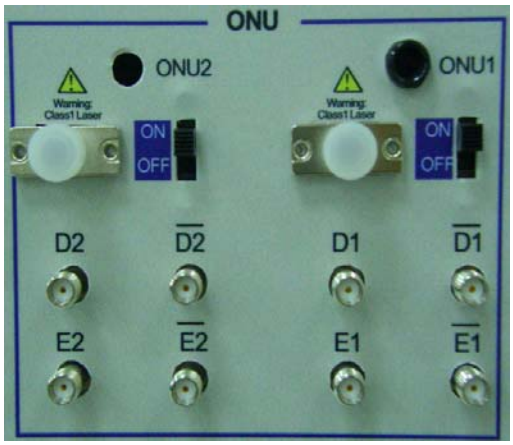
Panel Description

Front Panel Overview

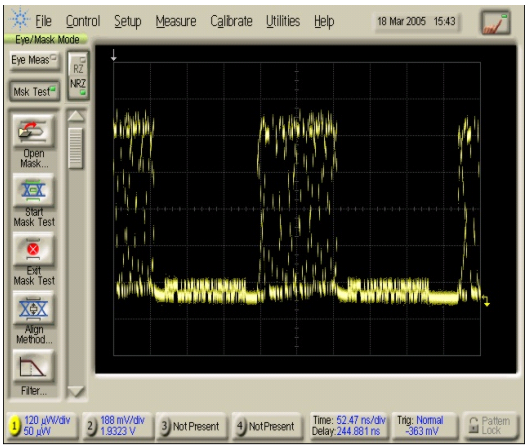


Rear Panel Overview

ONU Optical and Electrical I/F



(ONU1 & 2 Optical Burst Packets)



• **ONU Optical Transmitter**

Output Power： 0 ~ -2 dBm

LD Type： FP

Extinction Ratio (dB) ：9 (Typical)

Wavelength：1310nm (Typical)

Background DC light：<-45dBm

• **ONU Data output**

Bit Rate：155Mb/s to 1.25Gb/s

Format： NRZ

Type： Differential

Pattern： PRBS 7/23, All 0/1, PRGM

IEEE Test pattern (8B/10B), Idle1

Jitter Test Pattern (8B/10B),Idle 2

Level： 700mV

Tr/ Tf ：< 120ps

Port No.：2

Termination：+1.3V

• **Enable Timing Output**

Level：LVTTL

Termination：GND or +1.3V

Port No.：2 (Ch1 *1 , Ch2 *1)

Type：Differential

• **Clock Output**

Operation Frequency：155MHz to 1.25GHz

Level： 700mV

Tr/Tf： < 120ps

Port No.：1

Termination： AC-Couple

Type：Differential

Data/ Reset Output (for OLT Tx/Rx)

• **Data output** (OLT Tx)

Bit Rate：155Mb/s to 1.25Gb/s

Format：NRZ

Pattern：PRBS7/23, PRGM

IEEE Test Pattern (8B/10B)

Jitter Test Pattern (8B/10B)

Idle 1, 2 (8B/10B)

Termination：LVPECL (Vcc-1.3)

Type：Differential

• **Reset output**

Level：LVTTL

Termination：GND

Port No.：1

Type：Differential

OLT/ONU Data Input

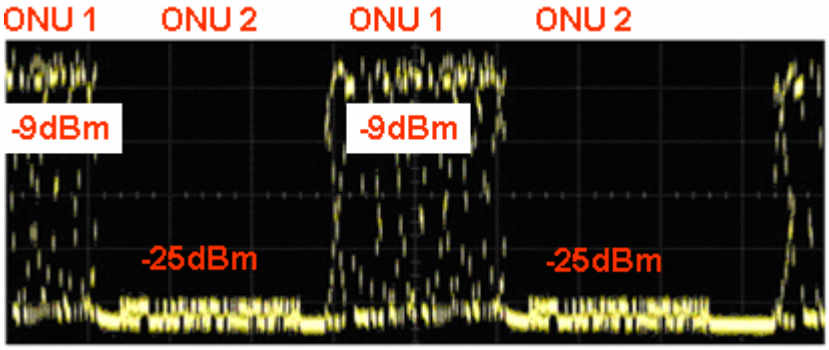
Data Input (OLT/ONU Rx)

Bit Rate：155Mb/s to 1.25Gb/s

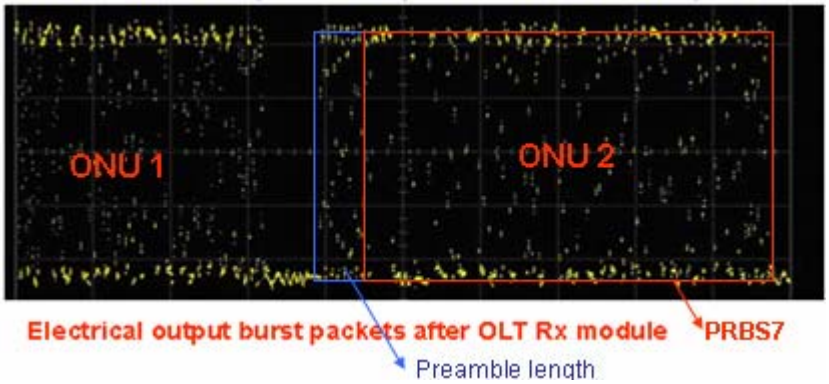
Input Range：1.755V~2.48V (DC Couple)

Sensitivity: < 400mVpp

Optical Burst Packets Input in OLT Rx



Electrical Burst Packets Output from OLT Rx



User Interface

The FMTS-PON User Interface is easily fitted to various PON measurement applications. The GUI interface provides the following functions

- Upstream/ Downstream Setup..... Tx/Rx
- Burst packet structure edition.....Tx (Preamble/ CID/ payload pattern size and type)
- Measurement area setting.....Rx
- Upstream control timing sequence set up....Tx
- Auto Phase/Threshold search.....Tx/Rx
- **Auto Gating alignment** .....Rx (Patent pending)
- Result Analysis

FMTS-PON provides two kinds of methodologies to compensate the delay between gating area and incoming data stream dealing with various kinds of delay.

1) **Auto** gating mechanism, it provides ±15 bits delay to synchronize / align the incoming data with specified gating area automatically.

2) **Manual** gating mechanism, system can allow operator to adjust the gating area with positive or negative direction and cooperate with error detector.

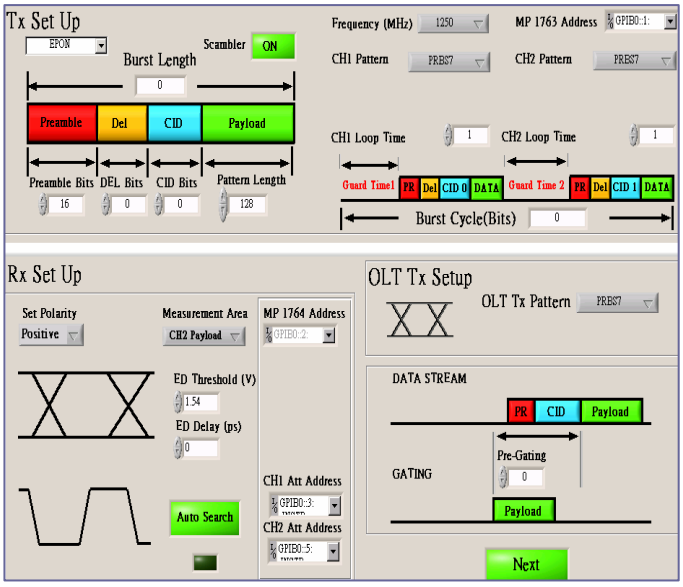


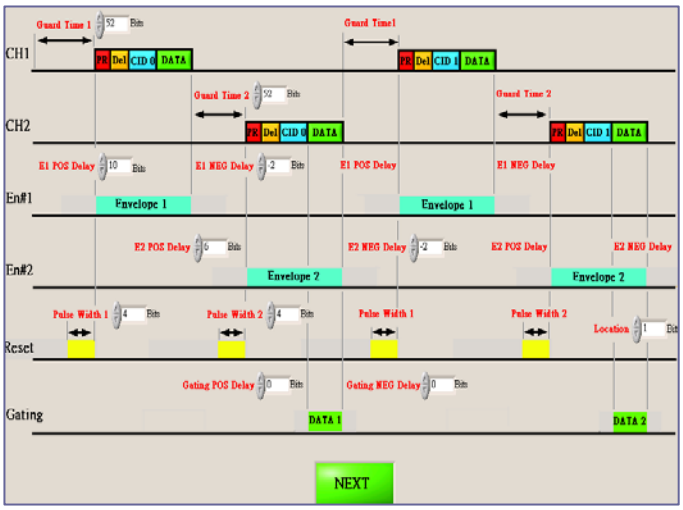
Figure 7：Frame Packet set up

Figure 8：Auto Gating Align and Synchronization

The system can align and synchronize the specified allocation area with incoming data stream within exceptionally short period automatically. (Figure 8)

The upstream timing generator allows simple access to each timing sequence via graphical instruction. (Figure 9)

User will be able to edit any specified payload patterns using notepad in Microsoft Windows or selecting pattern editor tool via PRGM sub-screen window and the pattern exporting form from pattern editor is text file. (Figure 10)



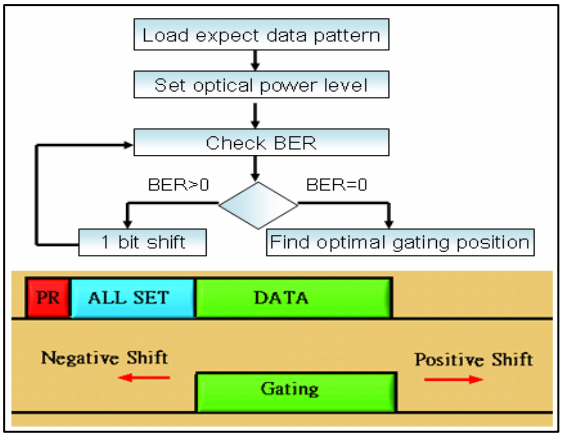


Figure 9：Timing sequence sub-screen

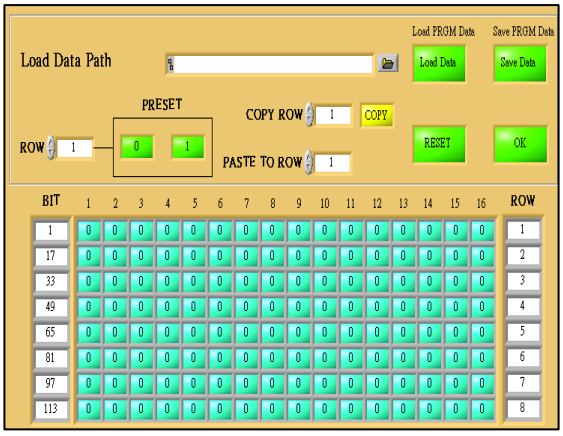


Figure 10: Pattern Editor

Mechanism of auto gating alignment

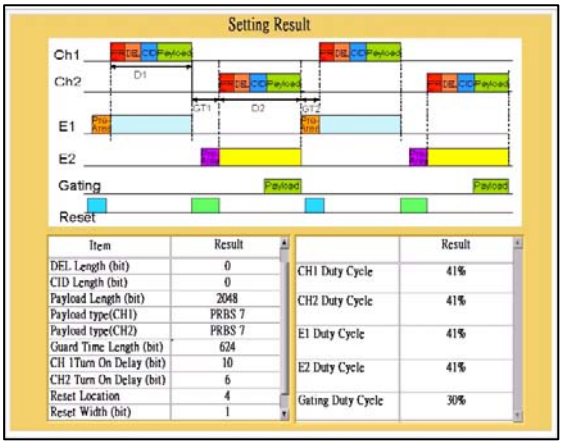


Figure 11: Setting result confirmation

Moving the gating position under specified power level and check the bit error rate till the BER =0 ,then active the auto search mechanism to make the optimal testing position automatically.

The FMTS-PON provide the summarization and display for setting result and calculate the duty cycle ratio for channel 1,channel 2, envelope 1, envelope 2 and gating channel.

Including calculate the bit density of channel 1 Channel 2 and receiving area locate on error detector.

Measurement Result Analysis / Minimum sensitivity analysis suit

The measuring analysis engine can provide the graphic table for BER versus input power、BER versus loud/soft ratio....etc. (Figure 12) Through the analysis function, it not only provides min. sensitivity measurement input by mono-channel signal, but also monitor the influence by adjacent channel power level., such as loud/soft ratio. (Figure 13)

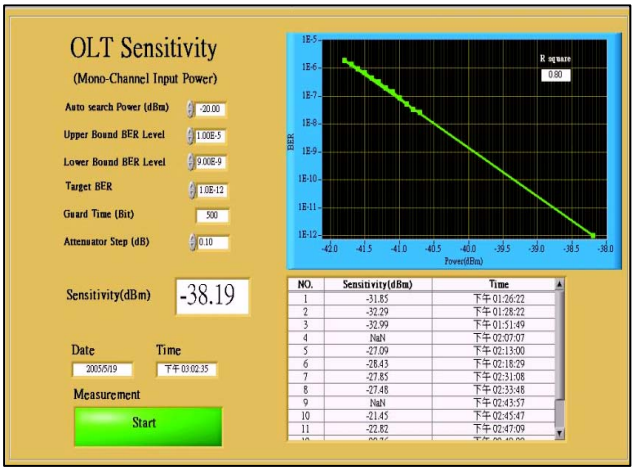


Figure 12：Min. Sensitivity Measurement

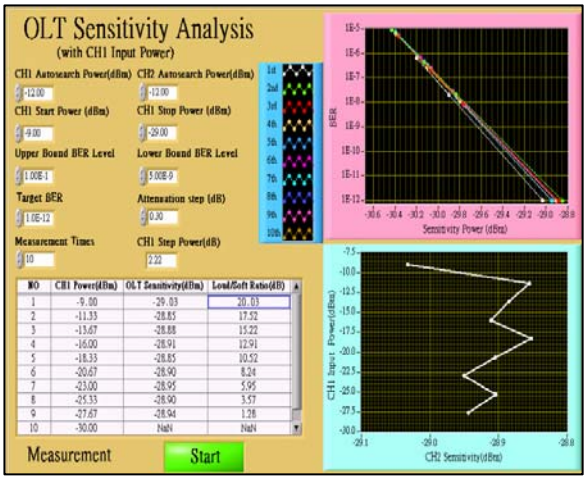


Figure 13：Min. sensitivity versus Loud/Soft Ratio

Connection Block Diagram of FMTS-PON

Downstream

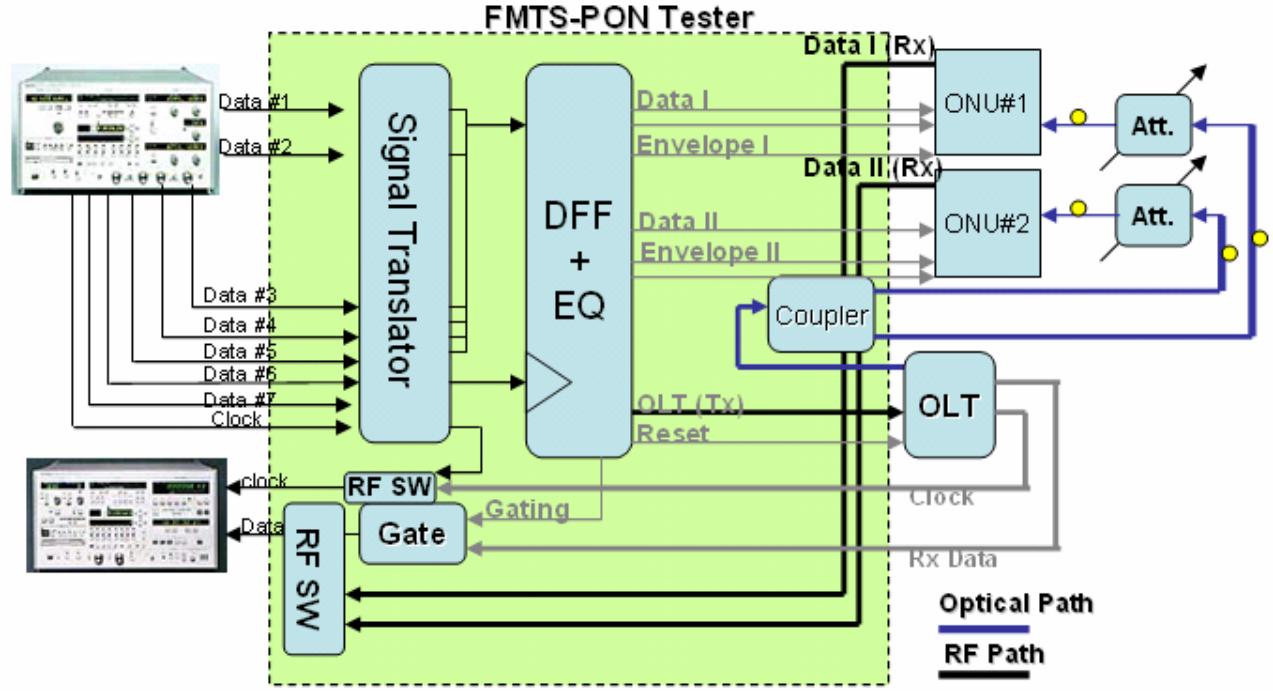


Figure 14：FMTS-PON Downstream connection block diagram

Upstream

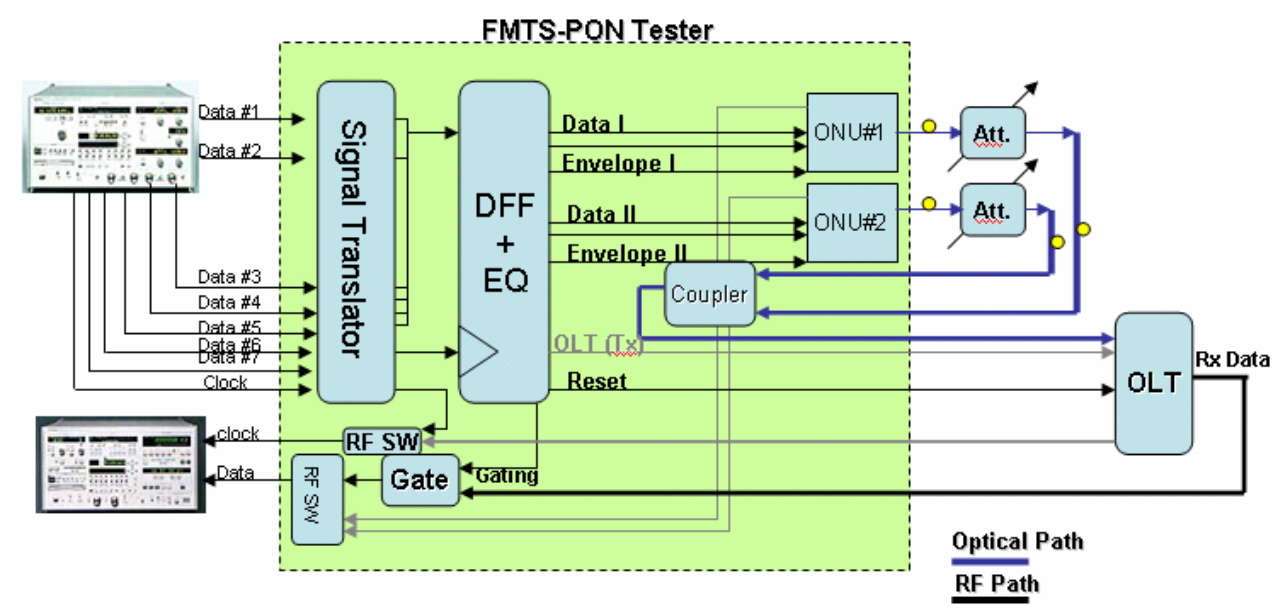


Figure 15：FMTS-PON Upstream connection block diagram

Multi-function Platform

FMTS-PON develop based Anritsu MP1763C/64C high speed and wide band bit error rate tester (BERT). It can fulfill various application, such as SONET/SDH (OC-3 to OC-192) with FEC coding , 3.125Gb/s x4、10.3125Gb/s in 10Gbit Ethernet ,1X,2x,4X ,8X and 10x Fiber Channel, Infini-band S-ATA and PCI Express for Next-Gen. PC peripheral I/F.....etc

Standard		Data Rate	Standard		Data Rate
Ethernet	10X	10.3125 Gb/s	**Infini-band**		2.5Gb/s
		1.25G Gb/s	**XAUI**		3.125Gb/s
Fiber Channel	1X	1.0625Gb/s	**Serial-ATA**	II	3.0Gb/s
	2X	2.0125Gb/s	**IEEE1394b**	4X	1.6Gb/s
	4X	4.25Gb/s		8X	3.2Gb/s
	8X	8.5Gb/s	**XFP**	XFI	9.9 to 11.2Gb/s
	10X	10.518 Gb/s			
SONET/SDH	OC-12/STM-4	622.08Mb/s			
	OC-48/STM-16	2.488Gb/s			
	OC-192(FEC)	9.953~10.7Gb/s			
PON	BPON	155~622Mb/s			
	EPON	1.25Gb/s			
	GPON	1.244~2.488Gb/s			

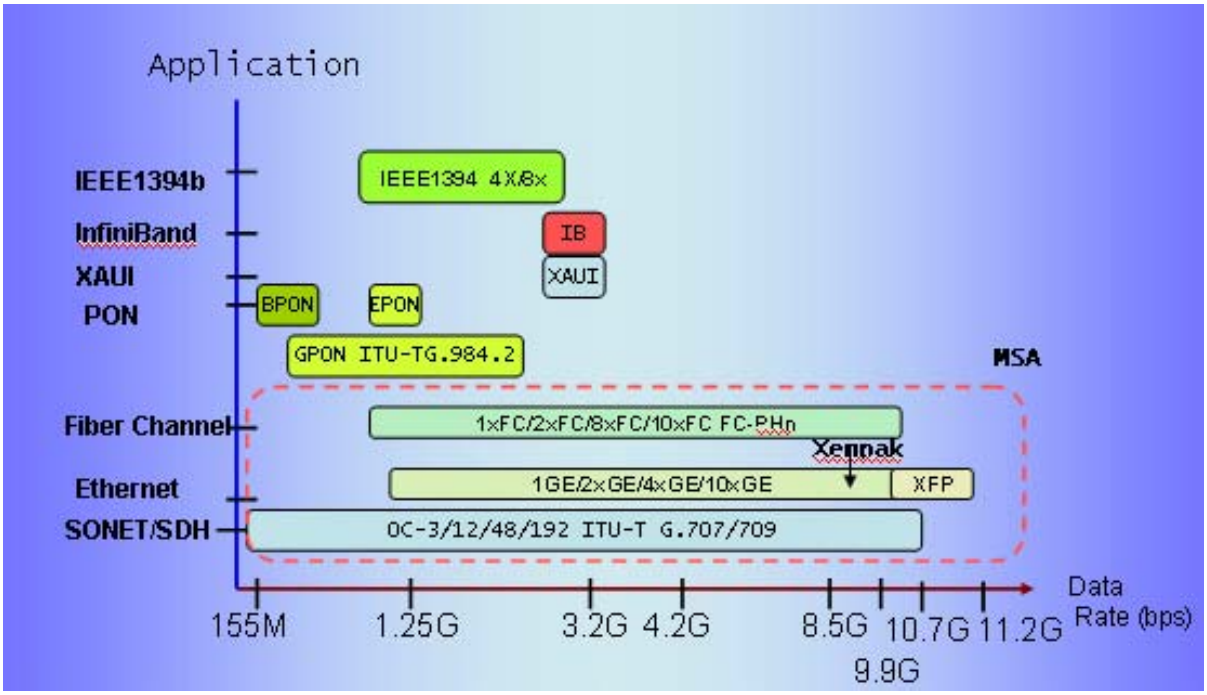


Figure 16: Various application fields for MP1763C/64C

Technical Specification

Table I：Electrical Specification

Items / Specification				Value
Operating Bit Rate (bps)				155M /622M/ 1250M
Input Signal (Rear)	Upstream	No. of ONU (Data)		2 Channels
		No. of Timing Control		4 Channels
	Downstream	OLT Transmitter (Data)		1 Channel
	Common	Clock		1 Channel
		Level		ECL
		Coupling Type		DC-Couple
		Termination		50Ω to -2V
		Connector		SMA female
Output Signal (Front)	Upstream Side	ONU#1/#2 Data	Number of Data	2 Pairs(LVPECL)
			Tr/Tf (20%~80%)	< 300ps
			Pattern Jitter	< 100ps
			Amplitude	> 500mV
			Type	Differential
		Envelope	Number	2 Pairs (LVTTL)
			Amplitude	> 500mV
			Type	Differential
		Reset	Number	1 Pair (LVTTL)
			Amplitude	> 500mV
			Type	Differential
	Downstream Side	Data (for OLT Tx)	Number	1 Pair (LVPECL)
			Amplitude	> 500mV
			Type	Differential
	Common	Clock	Number	1 Pair (AC couple)
			Type	Differential
		To ED Clock	Source Selection	From PPG Clock or OLT Clock are selectable
		To ED Data	Source Selection	From OLT/ONU#1/ONU#2 Data are selectable
		Termination		50Ω to +1.3V

Input Signal (Front)	Upstream	Data	Number	1 Channel (LVPECL)
			Circuit Coupling	AC / DC Couple Selectable on EV Board
			Max. DC Input Range	1.755V~2.48V @ 25°C (DC Couple)
			Input sensitivity	>400mVpp @ 25°C
			Type	Single Ended
	Downstream	ONU#1/#2	Data#1/#2	2 Channels (LVPECL)
			Input sensitivity	Refer to MP1764C spec.
	Common	Termination		50Ω to +1.3V
		Connector		SMA female
System Information		DC(+3.3V) Power Outlet		6 pairs
		AC Input Power Source		100 to 250 VAC 50/60Hz
		Power consumption		≤100W
		Operation Environment	Temp.	10~40°C
			Humidity	10%~85%
		EMI Filter		Embedded

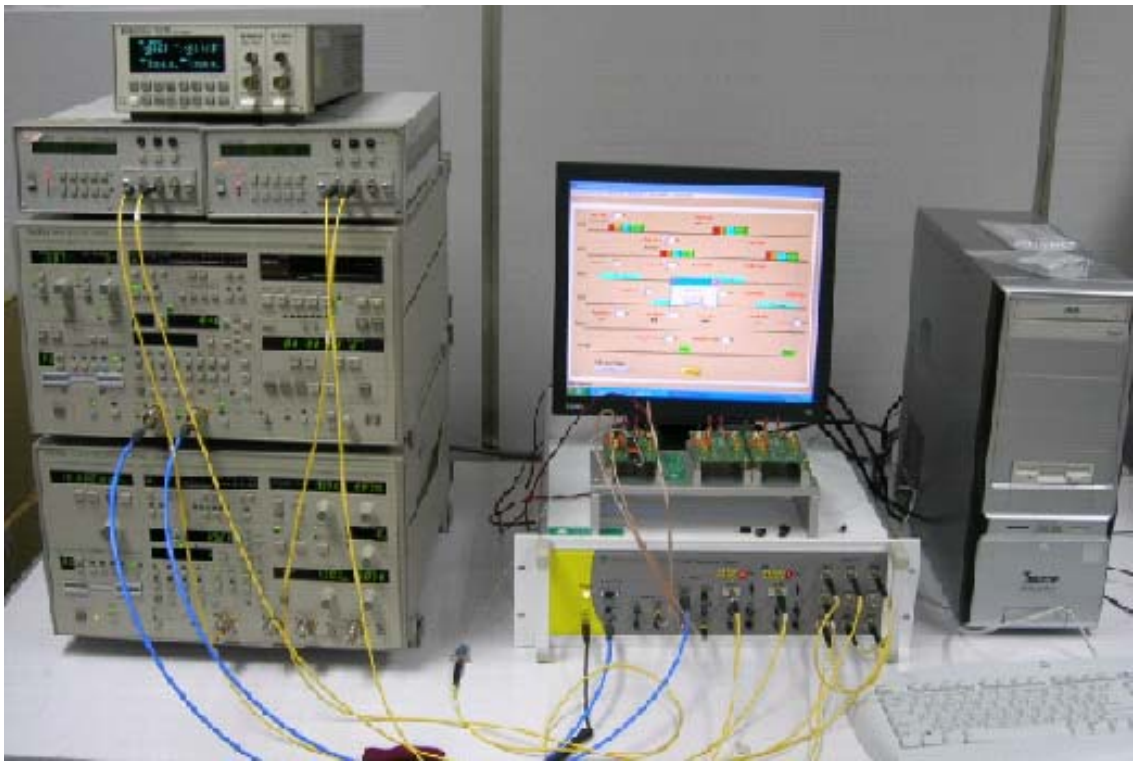


Table II： Software Environment Specification

Operation Mode		Upstream Mode / Downstream Mode	
Test Pattern Frame Structure		Payload Type *	PRBS 7,PRBS 23 /All 0, All 1 / PRGM /CRPAT/CJTPAT/ Idle 1,2
		Payload (bit)	128~65528 bits (16 bits/ step)
		Preamble Bit	0~2048 bits (2 bits/ step)
		Delimiter Bit	0~2048 bits (8 bits/ step)
		Consecutive Identical Digits	0~2048 bits “0” or “1”
		Pattern Resolution	8 bits
Scrambler		E-PON	Idle 1 Pattern
		G-PON	PRBS 7
Measurement Area	E-PON	Channel 1 Payload / Channel 2 Payload	
	G-PON	DEL+CID+ Channel 1 /2 Payload	
OLT Tx Test Pattern		PRBS7 / PRBS23 /All 0 , All1/ PRGM/ CRPAT/ CJTPAT/ Idle 1, Idle 2	
Control Timing Sequence		Alternative Loop Time	1~3 for Ch1 or Ch2
		Pre-Gating	± 256 Bits
		Guard Time	0 ~ 2048 bits (4 bits / Step)
		Burst Cycle	up to 1 M bits
		Envelope #1 width	Pattern length plus 0~16 bits
		Envelope #2 width	Pattern length plus 0~16 bits
		Reset width	≤ Guard Time bits
		Reset Location	0 ~ 128 bits (1 bit / Step)
		Gating Width	Payload Width plus 0~16 bits
Gating Alignment		Automatically	± 15 Bit
		Manually	± 64 bits
Background DC light		Channel 1 ON / OFF	Envelope 1 Full Low / High
		Channel 2 ON/ OFF	Envelope 2 Full Low / High
Continuous Mode		Channel 1	PRBS 7 / PRBS 23 / Idle 1, 2
		Channel 2	PRBS 7 / PRBS 23 / Idle 1, 2

* The payload of Ch1 & Ch2 can be set independently

* CRPAT, CJTPAT, Idle 1 and Idle 2 (8B/10B) are specified on IEEE802.3ah

Table III： Optical I/F Specification

Items / Specification		Value
WDM Coupler	Coupling Ratio	50%
	Number	1 pair
	Connector	FC/PC
Power Monitor	Coupling Ratio	99% & 1%
	Number	2 pairs
	Connector	FC/PC

Table IV： Optical Transmitter Specification

(10℃ < Operated Temp. < 40℃)

Items / Specification				Value
Optical I//F	Optical Output	Port No.		2 Port
		LD Type	ONU	FP
			OLT	DFB
		Output Power (dBm)		0 dBm (typically)
		Wavelength (nm)	ONU	1310 nm (typically)
			OLT	1490 nm (typically)
		Extinction Ratio (dB)		> 9
		Background Light		< - 45dBm (for ONU Tx)
		RIN		< -113 dBc/Hz
		Rise / Fall Time (20%~80%)		< 0.26 ns
		Total Jitter (p-p)		<0.1 ns

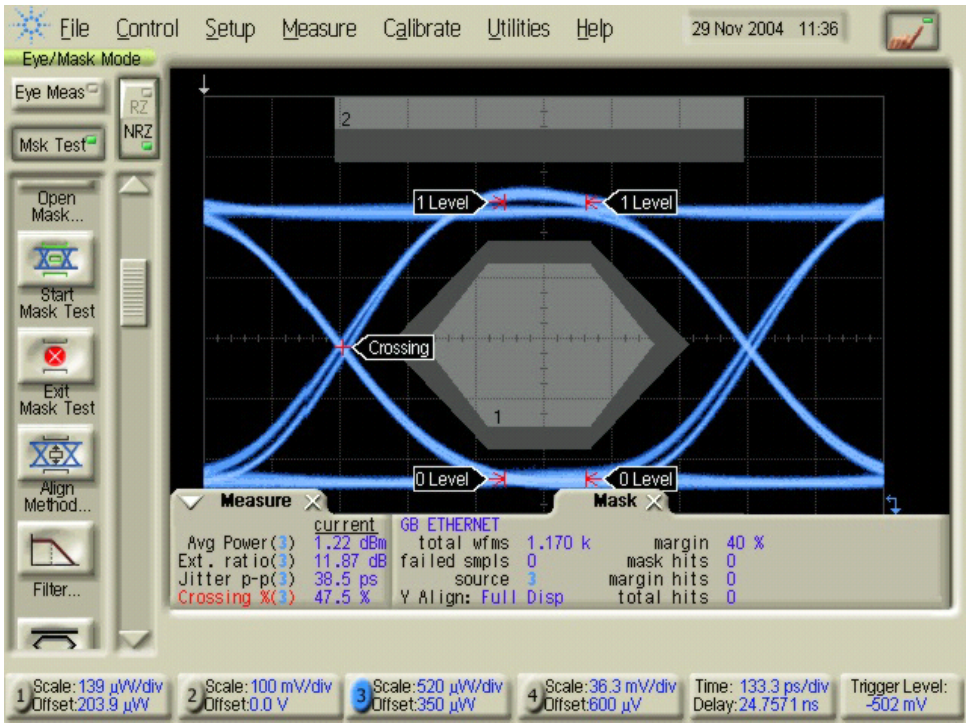


Figure 17：ONU Eye Diagram waveform

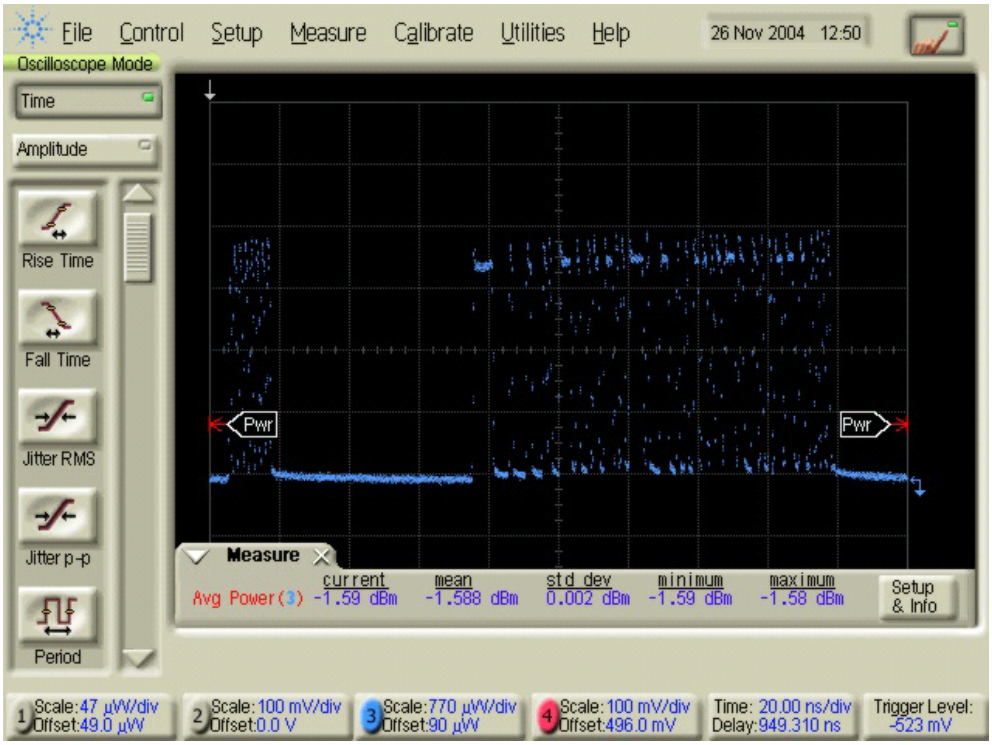
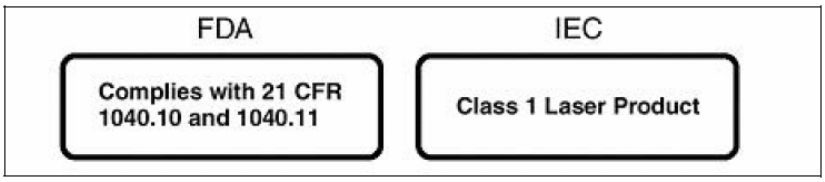


Figure 18：Burst Packet waveform generated by ONU



Laser Safety

The system provides two channels class 1 laser source. It complies with IEC60825 and FDA 21 CFR 1040.10 and 1040.11. The laser sources should be operated with the specified temperature and voltage limits and shall be terminated with optical connector or dust plug.

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Order Information

Model	Description	Qtn
	Main frame	
MP1763C	Pulse Pattern Generator (50MHz to 12.5GHz)	1
MP1763C-01	12.5GHz Synthesizer	1
MP1764C	Error Detector (50MHz to 12.5GHz)	1
FMTS-PON	Main Frame	1
FPON-HA9	SM Programmable Attenuator	2
	Standard Accessories	
FPON-E100	1 M SMA cable (M-M)	12
FPON-E40	0.4 M SMA cable (M-M)	8
FPON-E-Att-3	3dB Coaxial attenuator	1
FPON-O30	0.3 M SM fiber cable (FC-FC)	2
FPON-O100	1M SM fiber cable (FC-SC)	3
FPON-GPIB	IEEE488 GPIB cable (1M)	4
	SC-SC connector	2
	Wrist strap	1
	Control System	
FEECS	FMTS-PON Expert Evaluate Control Software	1

Specification subject to change without notice. Please contact Phytrex Corp. for further information. sales@phytrex.com